USBLC6-4SC6

ASD
(Application Specific Devices)

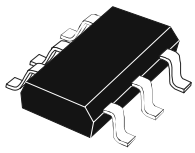
VERY LOW CAPACITANCE ESD PROTECTION

MAIN APPLICATIONS
- USB2.0 ports up to 480Mb/s (high speed)
- Backwards compatible with USB1.1 low and full speed
- Ethernet port: 10/100Mb/s
- SIM card protection
- Video line protection
- Portable electronics

DESCRIPTION
The **USBLC6-4SC6** is a monolithic Application Specific Discrete dedicated to ESD protection of high speed interfaces, such as USB2.0, Ethernet links and Video lines.
Its very low line capacitance secures a high level of signal integrity without compromising in protecting sensitive chips against the most stringent characterized ESD strikes.

FEATURES
- 4 data lines protection
- Protects V_{BUS}
- Very low capacitance: 3pF typ.
- SOT23-6L package
- RoHS compliant

BENEFITS
- Very low capacitance between lines to GND for optimized data integrity and speed
- Low PCB space consuming, 9mm² maximum foot print
- Enhanced ESD protection
- IEC61000-4-2 level 4 compliance guaranteed at device level, hence greater immunity at system level
- ESD protection of V_{BUS}. Allows ESD current flowing to Ground when ESD event occurs on data line
- High reliability offered by monolithic integration
- Low leakage current for longer operation of battery powered devices
- Fast response time
- Consistent D+ / D- signal balance:
  - Best capacitance matching tolerance I/O to GND = 0.015pF
  - Compliant with USB 2.0 requirements < 1pF



SOT23-6L

Figure 1: Functional Diagram

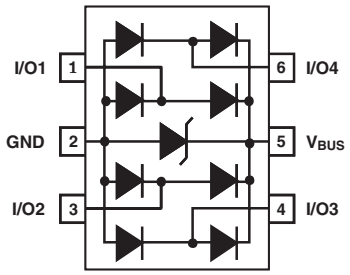


Table 1: Order Code

Part Number	Marking
USBLC6-4SC6	UL46

COMPLIES WITH THE FOLLOWING STANDARDS:
- IEC61000-4-2 level4:
  - 15kV (air discharge)
  - 8kV (contact discharge)

Table 2: Absolute Ratings

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	At device level: IEC61000-4-2 air discharge IEC61000-4-2 contact discharge MIL STD883C-Method 3015-6	 15 15 25	kV
T_{stg}	Storage temperature range		-55 to +150	°C
T_j	Maximum junction temperature		125	°C
T_L	Lead solder temperature (10 seconds duration)		260	°C

Table 3: Electrical Characteristics (T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{RM}	Reverse stand-off voltage				5	V
I_{RM}	Leakage current	V_{RM} = 5V			2	µA
V_{BR}	Breakdown voltage between V_{BUS} and GND	I_R = 1mA	6			V
V_F	Forward voltage	I_R = 10mA			0.86	V
V_{CL}	Clamping voltage	I_{PP} = 1A, t_p = 8/20µs Any I/O pin to GND			12	V
		I_{PP} = 5A, t_p = 8/20µs Any I/O pin to GND			17	V
$C_{i/o-GND}$	Capacitance between I/O and GND	V_R = 1.65V		3	4	pF
$\Delta C_{i/o-GND}$				0.015		
$C_{i/o-i/o}$	Capacitance between I/O	V_R = 1.65V		1.85	2.7	pF
$\Delta C_{i/o-i/o}$				0.04		

Figure 2: Capacitance versus voltage (typical values)

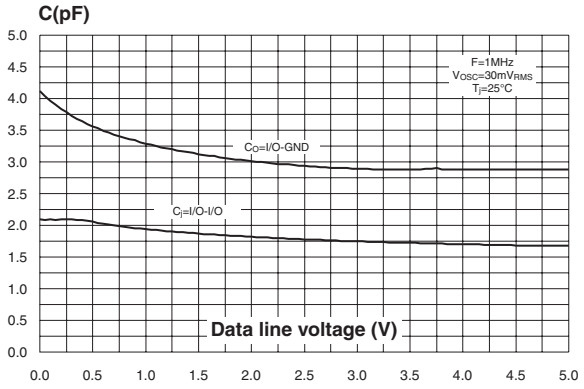


Figure 3: Line capacitance versus frequency (typical values)

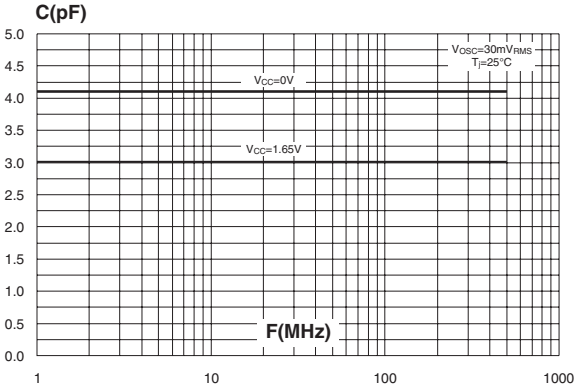


Figure 4: Relative variation of leakage current versus junction temperature (typical values)

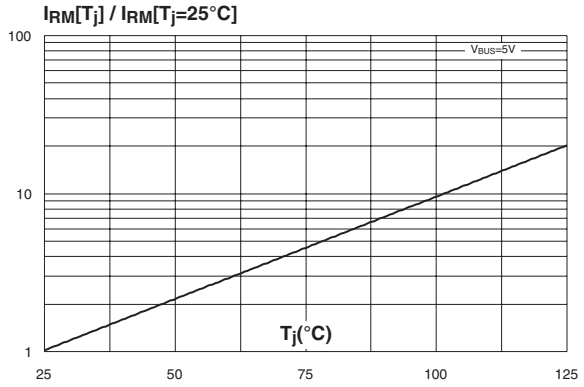
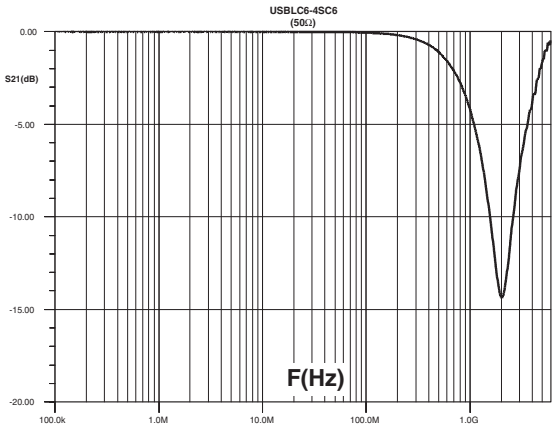


Figure 5: Frequency response



TECHNICAL INFORMATION

1. SURGE PROTECTION

The USBLC6-4SC6 is particularly optimized to perform surge protection based on the rail to rail topology. The clamping voltage V_{CL} can be calculated as follow :

$V_{CL}+ = V_{BUS} + V_F$ for positive surges

$V_{CL}- = - V_F$ for negative surges

with: $V_F = V_T + R_d.I_p$

(V_F forward drop voltage) / (V_T forward drop threshold voltage)

We assume that the value of the dynamic resistance of the clamping diode is typically:

$R_d = 1.4\Omega$ and $V_T = 1.2V$.

For an IEC61000-4-2 surge Level 4 (Contact Discharge: V_g=8kV, R_g=330Ω), V_{BUS} = +5V, and if in first approximation, we assume that : $I_p = V_g / R_g = 24A$.

So, we find:

$V_{CL}+ = +39V$

$V_{CL}- = -34V$

Note: the calculations do not take into account phenomena due to parasitic inductances.

2. SURGE PROTECTION APPLICATION EXAMPLE

If we consider that the connections from the pin V_{BUS} to V_{CC} and from GND to PCB GND are done by two tracks of 10mm long and 0.5mm large; we assume that the parasitic inductances Lw of these tracks are about 6nH. So when an IEC61000-4-2 surge occurs, due to the rise time of this spike (tr=1ns), the voltage V_{CL} has an extra value equal to Lw.dI/dt.

The dI/dt is calculated as: dI/dt = Ip/tr = 24 A/ns

The overvoltage due to the parasitic inductances is: Lw.dI/dt = 6 x 24 = 144V

By taking into account the effect of these parasitic inductances due to unsuitable layout, the clamping voltage will be :

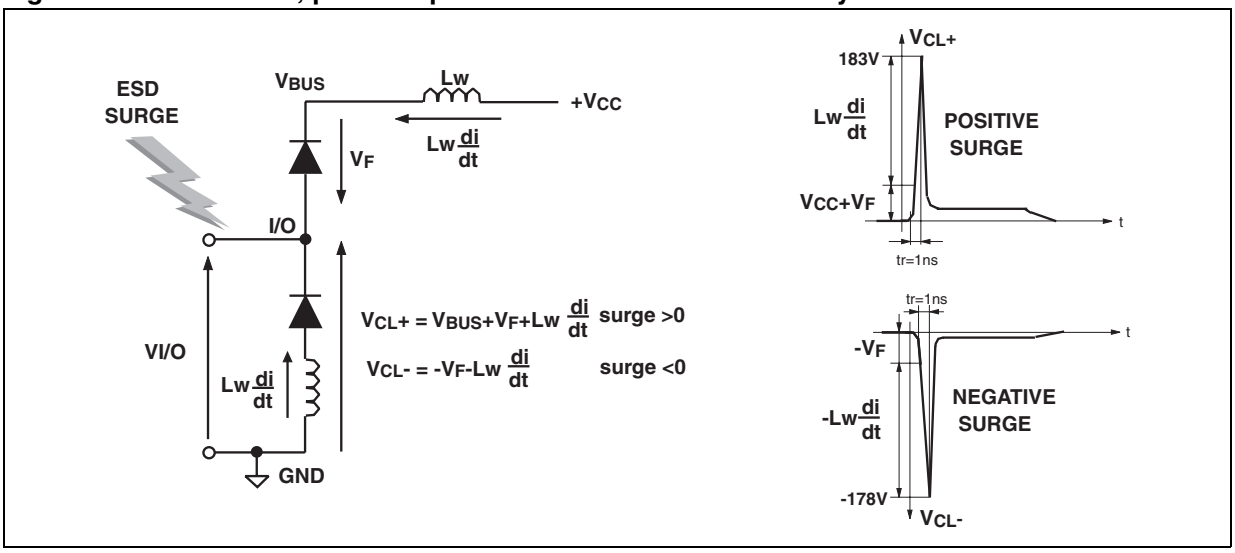
$V_{CL}+ = +39 + 144 = 183V$

$V_{CL}- = -34 - 144 = -178V$

We can reduce as much as possible these phenomena with simple layout optimization.

It's the reason why some recommendations have to be followed (see paragraph "How to ensure a good ESD protection").

Figure 6: ESD behavior; parasitic phenomena due to unsuitable layout



3. HOW TO ENSURE A GOOD ESD PROTECTION

While the USBLC6-4SC6 provides a high immunity to ESD surge, an efficient protection depends on the layout of the board. In the same way, with the rail to rail topology, the track from the V_{BUS} pin to the power supply $+V_{CC}$ and from the V_{BUS} pin to GND must be as short as possible to avoid overvoltages due to parasitic phenomena (see figure 6).
It's often harder to connect the power supply near to the USBLC6-4SC6 unlike the ground thanks to the ground plane that allows a short connection.

To ensure the same efficiency for positive surges when the connections can't be short enough, we recommend to put close to the USBLC6-4SC6, between V_{BUS} and ground, a capacitance of 100nF to prevent from these kinds of overvoltage disturbances (see figure 7).
The add of this capacitance will allow a better protection by providing during surge a constant voltage.
The figures 8, 9 and 10 show the improvement of the ESD protection according to the recommendations described above.

Figure 7: ESD behavior: optimized layout and add of a capacitance of 100nF

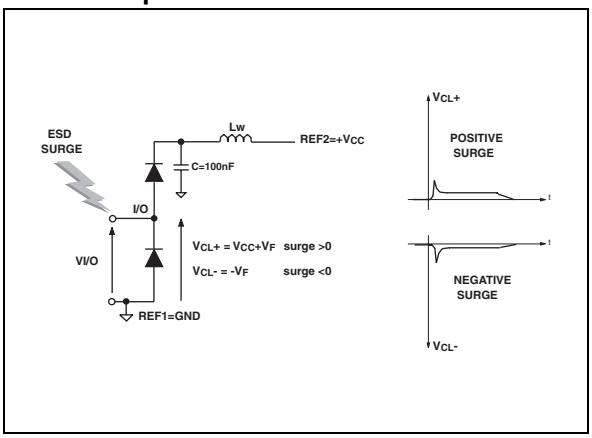


Figure 8: ESD behavior: measurements conditions (with coupling capacitance)

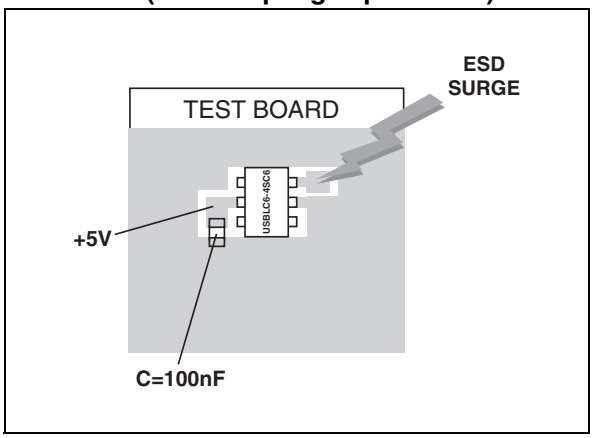


Figure 9: Remaining voltage after the USBLC6-4SC6 during positive ESD surge

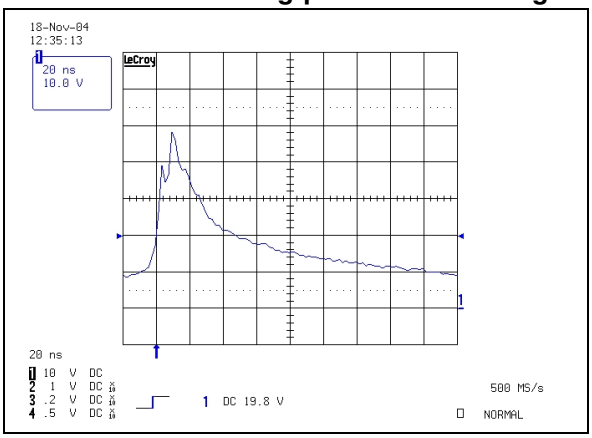
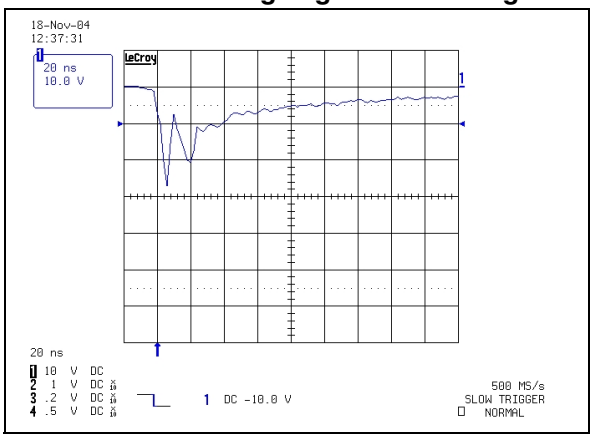


Figure 10: Remaining voltage after the USBLC6-4SC6 during negative ESD surge



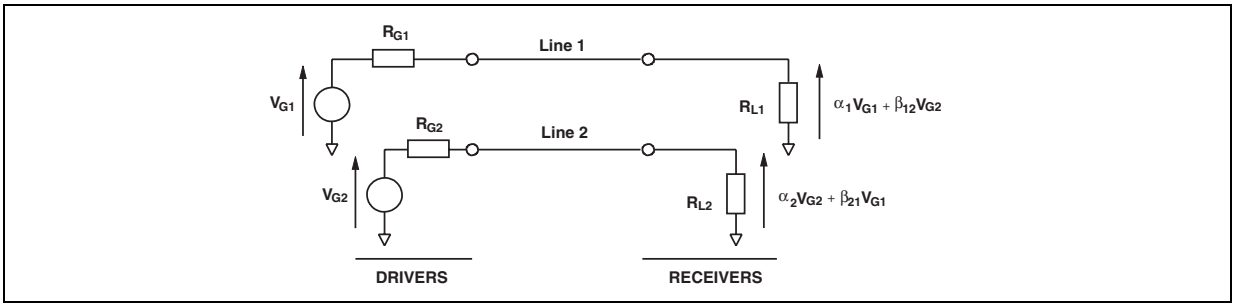
IMPORTANT:
A main precaution to take is to put the protection device closer to the disturbance source (generally the connector).

Note: The measurements have been done with the USBLC6-4SC6 in open circuit.

4. CROSSTALK BEHAVIOR

4.1. Crosstalk phenomena

Figure 11: Crosstalk phenomena



The crosstalk phenomena are due to the coupling between 2 lines. The coupling factor (β12 or β21) increases when the gap across lines decreases, particularly in silicon dice. In the example above the expected signal on load R_{L2} is $\alpha_2 V_{G2}$, in fact the real voltage at this point has got an extra value $\beta_{21} V_{G1}$. This part of the V_{G1} signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ).

Figure 12: Analog crosstalk measurements

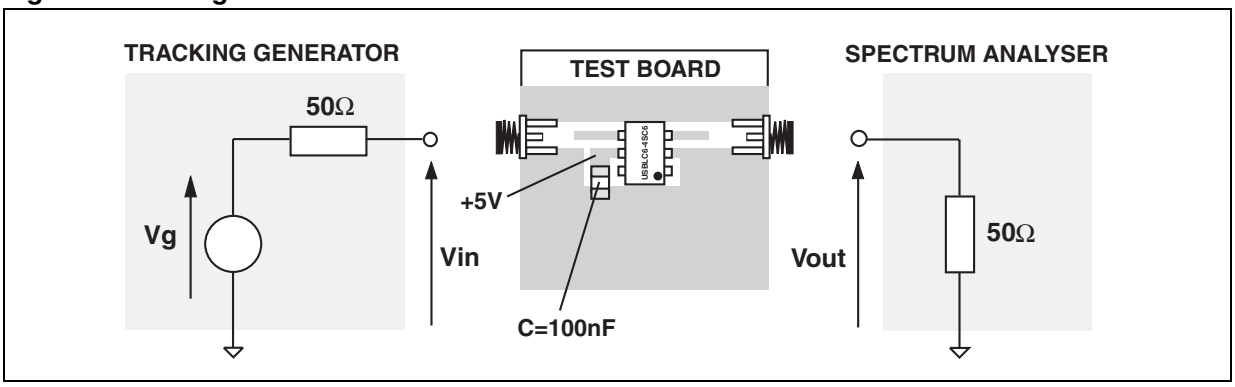
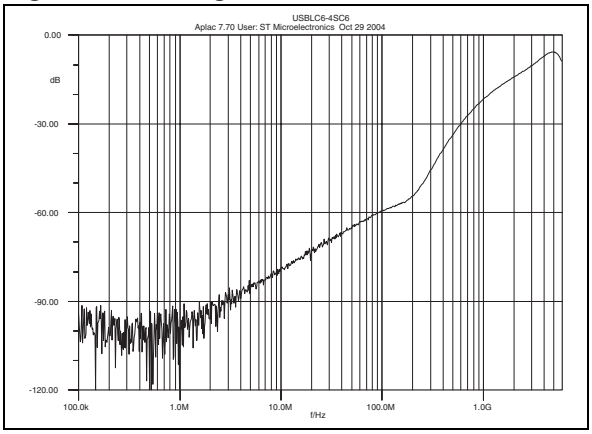


Figure 12 gives the measurement circuit for the analog application. In usual frequency range of analog signals (up to 240MHz) the effect on disturbed line is less than -55 dB (please see figure 13).

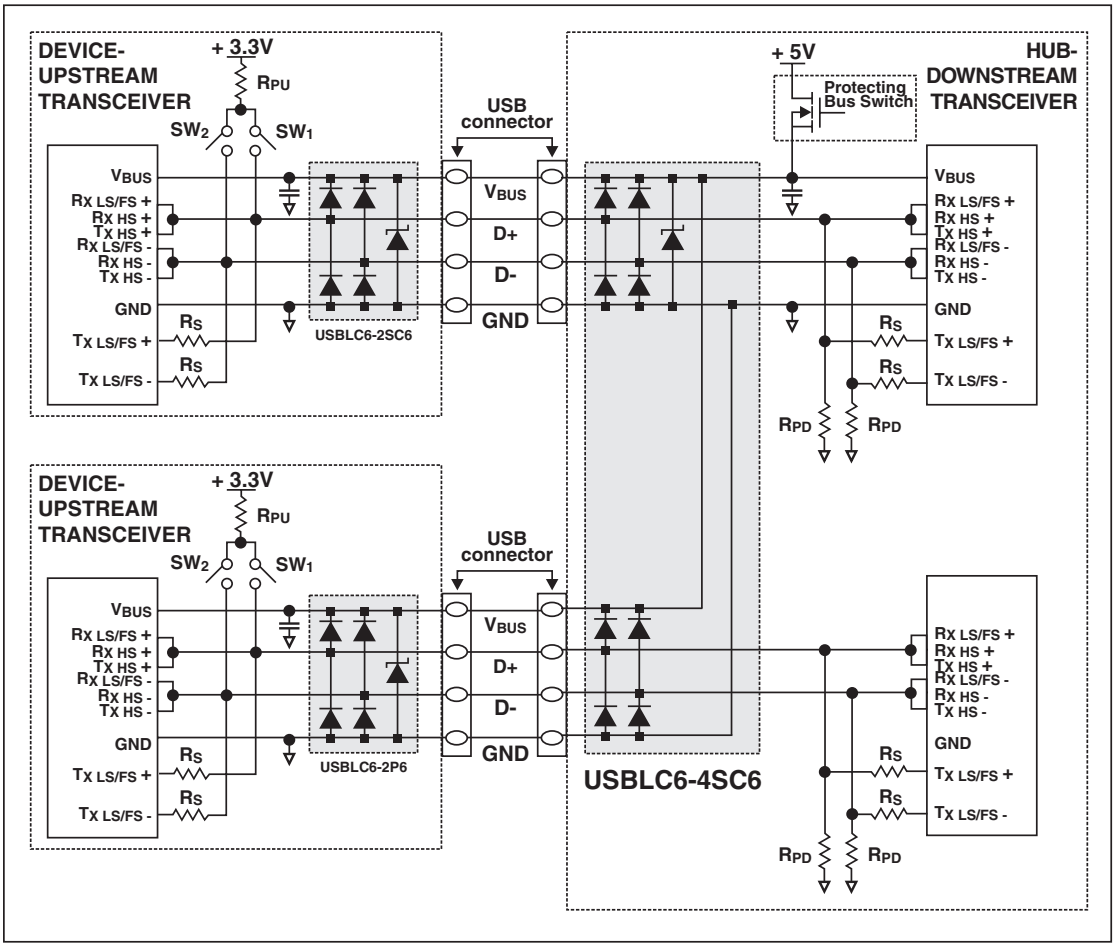
Figure 13: Analog crosstalk results



As the USBLC6-4SC6 is designed to protect high speed data lines, it must ensure a good transmission of operating signals. The frequency response (figure 5) gives attenuation information and shows that the USBLC6-4SC6 is well suitable for data line transmission up to 480 Mbit/s while it works as a filter for undesirable signals like GSM (900MHz) frequencies, for instance.

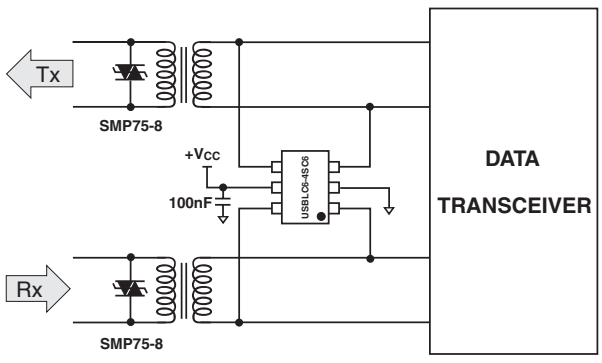
5. APPLICATION EXAMPLES

Figure 14: USB2.0 port application diagram using USBLC6-4SC6



Mode	SW_1	SW_2
Low Speed LS	Open	Closed
Full Speed FS	Closed	Open
High Speed HS	Closed then open	Open

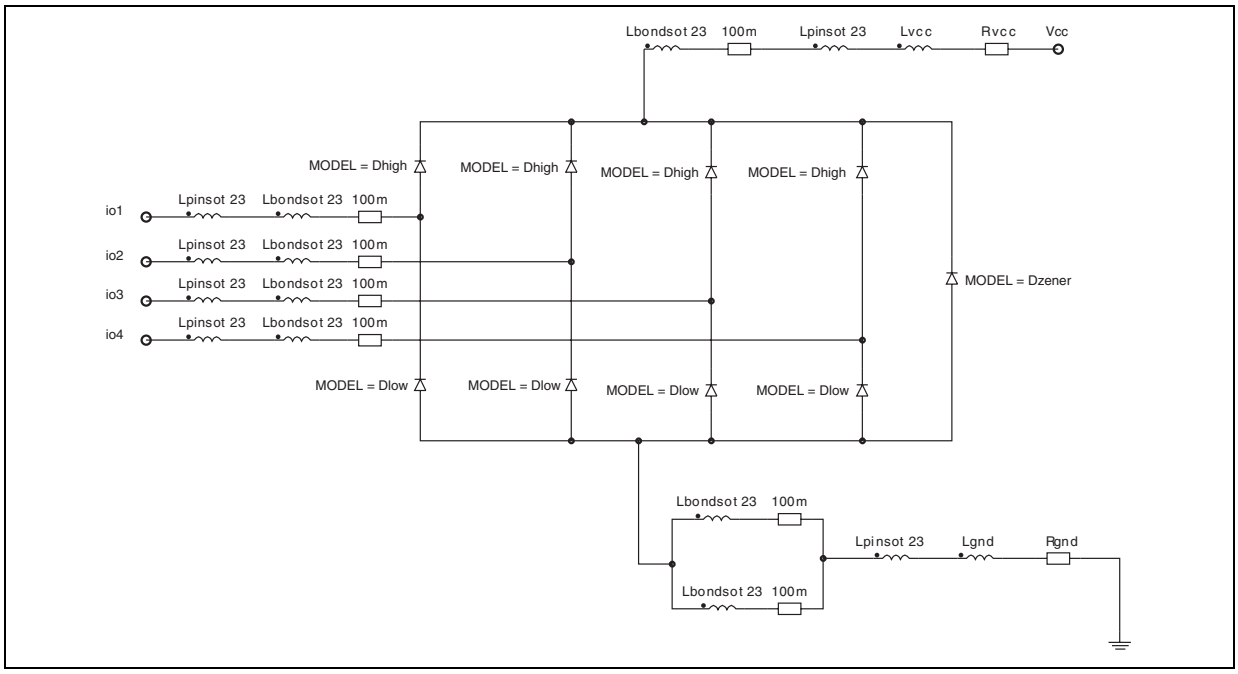
Figure 15: T1/E1/Ethernet protection



6. PSPICE MODEL

Figure 16 shows the PSPICE model of one USBLC6-4SC6 cell. In this model, the diodes are defined by the PSPICE parameters given in figure 17.

Figure 16: PSPICE model



Note: This simulation model is available only for an ambient temperature of 27°C.

Figure 17: PSPICE parameters

	Dlow	Dhigh	Dzener
BV	50	50	7.3
CJ0	2.4p	2.4p	20p
IBV	1m	1m	1m
IKF	0.038	0.018	2.42
IS	55.2p	2.27f	3.21p
ISR	100p	100p	100p
N	1.62	1.13	1.24
M	0.3333	0.3333	0.3333
RS	0.38	0.63	0.42
VJ	0.6	0.6	0.6
TT	0.1u	0.1u	0.1u

Lbondsot23	0.564n
Lpinsot23	0.15n
Rgnd	350m
Lgnd	100p
Rvcc	350m
Lvcc	100p

Figure 18: USBLC6-4SC6 PCB layout considerations

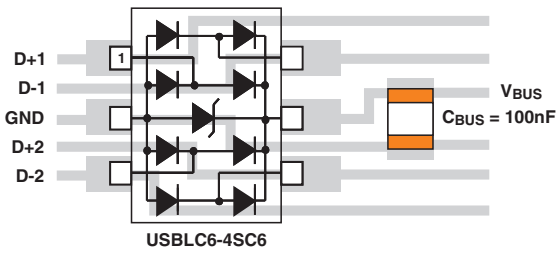
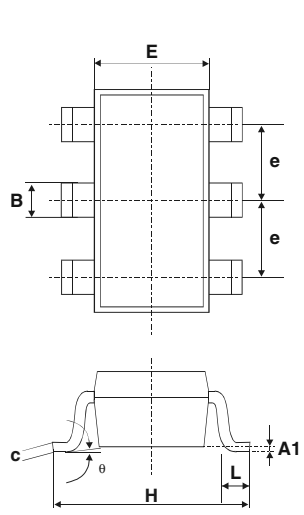
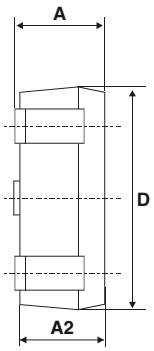


Figure 19: SOT23-6L Package Mechanical Data





REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1	0		0.10	0		0.004
A2	0.90		1.30	0.035		0.051
b	0.35		0.50	0.014		0.02
C	0.09		0.20	0.004		0.008
D	2.80		3.05	0.110		0.120
E	1.50		1.75	0.059		0.069
e		0.95			0.037	
H	2.60		3.00	0.102		0.118
L	0.10		0.60	0.004		0.024
θ	0°		10°	0°		10°

Figure 20: Foot Print Dimensions (in millimeters)

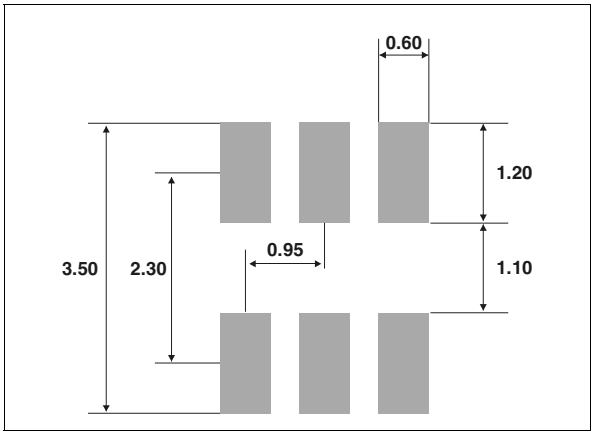


Table 4: Ordering Information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
USBLC6-4SC6	UL46	SOT23-6L	16.7 mg	3000	Tape & reel

Table 5: Revision History

Date	Revision	Description of Changes
10-Dec-2004	1	First issue.
28-Feb-2005	2	Minor layout update. No content change.

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